CLAIMS

What is claimed is:

1   1.   An apparatus comprising:

2   a first adder to add a first branch metric value to a previous path metric

3   value to generate a first path metric value; and

4   saturating logic to detect a saturating condition when a most significant bit

5   ("MSB") of said first path metric value is a specified value and to responsively

6   substitute a predetermined maximum value for said first path metric value.

1   2.   The apparatus as in claim 1 further comprising:

2   a comparator to compare said first path metric value or said

3   predetermined maximum value with a second path metric value or said

4   predetermined maximum value transmitted from a second adder, and to

5   responsively select a minimum one of said values.

1   3.   The apparatus as in claim 2 further comprising:

2   an accumulator to store said minimum one of said values for subsequent

3   path metric calculations.

1   4.   The apparatus as in claim 1 wherein said saturating logic comprises:

2   a multiplexer to select between said predetermined maximum value and

3   said new path metric value, wherein said value of said MSB operates as

4   selection logic to said multiplexer.

1   5.   The apparatus as in claim 3 wherein said predetermined maximum

2   value is a maximum value that may be stored by said accumulator.

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1   9. The apparatus as in claim 1 wherein said predetermined maximum

2   value is 7h7f.

1   5. The apparatus as in claim 2 further comprising:

2   a plurality of additional comparators to compare path metric values and

3   select a minimum for a plurality of additional accumulators.

1   6. The apparatus as in claim 5 wherein the total number of accumulators

2   is equal to a Viterbi trellis depth.

1   7. The apparatus as in claim 5 wherein the total number of accumulators

2   is equal to 64.

1   10. A computer-implemented method comprising:

2   adding a first branch metric value to a previous path metric value to

3   generate a first path metric value; and

4   detecting a saturating condition when a most significant bit ("MSB") of said

5   first path metric value is a specified value; and

6   responsively substituting a predetermined maximum value for said first

7   path metric value.

1   11. The method as in claim 10 further comprising:

2   comparing said first path metric value or said predetermined maximum

3   value with a second path metric value or said predetermined maximum value

4   transmitted from a second adder; and

5   responsively selecting a minimum one of said values.

1   12. The method as in claim 11 further comprising:

2   storing said minimum one of said values for subsequent path metric

3   calculations.

1   16. The method as in claim 10 wherein substituting comprises:

2   configuring a multiplexer to select between said predetermined maximum

3   value and said new path metric value, wherein said value of said MSB operates

4   as selection logic to said multiplexer.

1   13. The method as in claim 12 wherein said predetermined maximum

2   value is a maximum value that may be stored by said accumulator.

1   17. The method as in claim 10 wherein said predetermined maximum

2   value is 7h7f.

1   14. The method as in claim 12 further comprising:

2   comparing path metric values and selecting a minimum for a plurality of

3   additional accumulators.

1   15. The method as in claim 14 wherein the total number of accumulators

2   is equal to a Viterbi trellis depth.

1   18. The method as in claim 10 wherein the total number of accumulators

2   is equal to 64.

1   19. A machine-readable medium having code stored thereon which

2   defines an integrated circuit (IC), said IC comprising:

3   a first adder to add a first branch metric value to a previous path metric

4   value to generate a first path metric value; and

5   saturating logic to detect a saturating condition when a most significant bit

6   ("MSB") of said first path metric value is a specified value and to responsively

7   substitute a predetermined maximum value for said first path metric value.

1   20. The machine-readable medium as in claim 19 further comprising:

2   a comparator to compare said first path metric value or said

3   predetermined maximum value with a second path metric value or said

4   predetermined maximum value transmitted from a second adder, and to

5   responsively select a minimum one of said values.

1   21. The machine-readable medium as in claim 20 wherein said IC further

2   comprises:

3   an accumulator to store said minimum one of said values for subsequent

4   path metric calculations.

1   26
     22. The machine-readable medium as in claim 19 wherein said saturating

2   logic comprises:

3   a multiplexer to select between said predetermined maximum value and

4   said new path metric value, wherein said value of said MSB operates as

5   selection logic to said multiplexer.

1   *22*

1   28. The machine-readable medium as in claim 21 wherein said

2   predetermined maximum value is a maximum value that may be stored by said

3   accumulator.

1   *27*

1   24. The machine-readable medium as in claim 19 wherein said

2   predetermined maximum value is 7h7f.

1   *23*

1   25. The machine-readable medium as in claim 20 wherein said IC further

2   comprising:

3   a plurality of additional comparators to compare path metric values and

4   select a minimum for a plurality of additional accumulators.

1   *24*   *23*

1   26. The machine-readable medium as in claim 25 wherein the total

2   number of accumulators is equal to a Viterbi trellis depth.

1   *25*   *23*

1   27. The machine-readable medium as in claim 25 wherein the total

2   number of accumulators is equal to 64.